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10/072,931	02/12/2002	Shunpei Yamazaki	740756-2433	3751

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,931	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-85* is/are pending in the application.

4a) Of the above claim(s) *See Continuation Sheet* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *See Continuation Sheet* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/27/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims withdrawn from consideration are 1-9,12,14,16,18,20,22,24,26,28,30,32,34,36,38,40,42,44,46,48,50,52,54,56,58,60,62,64,66,68,70,72,74 and 76.

Continuation of Disposition of Claims: Claims rejected are 10,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39,41,43,45,47,49,51,53,55,57,59,61,63,65,67,69,71,73,75 and 77-85.

DETAILED ACTION

This Office Action is in response to the amendment filed on 2/21/06. Currently, claims 1-85 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 2/27/06 was filed after the mailing date of the Office Action on 11/16/05. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

The rejection of claims 10,13, 15, 17, 25, 27, 29, 33, 35, 37, 39, 41, 47, 49, 51, 53, 55, 57, 63, 65, 67, 69, 71, 73 and 77-80 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Yamazaki et al., claims 20-24, 27-31, 33 and 35, of U.S. Patent No. 6, 808,968. Although the conflicting claims are not identical, they are not patentably

distinct from each other because the current application (10/072,931) anticipates the limitations of Yamazaki et al., US Patent 6,808,968 is maintained for reasons of record.

Pertaining to independent claims 10, 47, 49, 67 and 78 of the current application (10/072,931), Yamazaki shows the invention substantially as claimed. See, claim 20, where Yamazaki shows, a method of manufacturing a semiconductor device comprising the steps of: adding a metal element to a first semiconductor film comprising amorphous silicon over a substrate; crystallizing the first semiconductor film to form a first crystalline semiconductor film; forming a barrier layer on the first crystalline semiconductor film; forming a second semiconductor film on the barrier layer; reducing a concentration of the metal element in the first crystalline semiconductor film by allowing the upper layer of the second semiconductor film to getter the metal element; and removing the second semiconductor film. In addition, pertaining to dependent claim 13 of the current application (10/072,931), Yamazaki shows in claim 22, wherein the second semiconductor film has an amorphous structure or a crystalline structure. Also, pertaining to dependent claim 15 of the current application (10/072,931), Yamazaki shows in claim 23, wherein the metal element is at least one element selected from the group consisting of Fe, Ni, Co, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au. Pertaining to dependent claim 17 of the current application (10/072,931), Yamazaki shows in claim 24, wherein the crystallizing step s carried out by a heat treatment. In addition, pertaining to dependent claims 23, 51 and 69 of the current application (10/072,931), Yamazaki shows in claim 27, wherein the barrier layer is formed by oxidizing the surface of the first crystalline semiconductor film with a solution containing ozone. Also, pertaining to dependent claims 25, 53 and 71 of the current application (10/072,931), Yamazaki shows in claim 28, wherein the barrier layer is formed by oxidizing the surface of the

first crystalline semiconductor film by an ultraviolet irradiation. Pertaining to dependent claim 27 of the current application (10/072,931), Yamazaki shows in claim 29, wherein the reducing step is carried out by a heat treatment. In addition, pertaining to dependent claim 29 of the current application (10/072,931), Yamazaki shows in claim 30 wherein the reducing step is carried out by irradiating the first crystalline semiconductor film with a light. Also, pertaining to dependent claims 33, 35, 37 and 39 of the current application (10/072,931), Yamazaki shows in claim 33, wherein the light is emitted from one selected form the group consisting of a halogen lamp, metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, and a high pressure mercury lamp. Pertaining to claims 41, 55, 57, 73 and 79 of the current application (10/072,931), Yamazaki shows in claim 21, further comprising a step of adding at least one element selected from the group consisting of He, Ne, Ar, Kr, Xe, O, O2, H and H2 to the second semiconductor film. In addition, pertaining to claims 63, 65 and 77 of current application (10/072,931), Yamazaki shows in claim 35 wherein the semiconductor device is at least one selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle-type display, a player using a recording medium, a digital camera, a projector, a mobile phone and portable book.

However, Yamazaki fails to show, pertaining to the independent claims 10, 47, 49, 67 and 78 of the current application (10/072,931), "adding a noble gas element to a region of the (second) semiconductor film."

Yamazaki teaches, in the independent claim 20, "adding one conductive type impurity element to only an upper layer of the second semiconductor film". In addition, Yamazaki teaches in the dependent claim 21, "further comprising a step of adding at least one element

selected from the group consisting of He, Ne, Ar, Kr, Xe, O, O2, H, and H2 to the second semiconductor film."

It would have been obvious to one of ordinary skill in the art to incorporate, adding a noble gas element, in the current application (10/072,931), according to the teaching of Yamazaki, with the motivation that, Yamazaki includes adding at least one element selected from the group consisting of He, Ne, Ar, Kr, Xe, where theses element represent specific noble gas elements.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The rejection of claims 10, 11 13, 15, 17, 19, 21, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 49, 53, 55, 57, 59, 61, 63, 65, 67, 71, 73, 75 and 77-85 under 35 U.S.C. 103(a) as being obvious over Yamazaki et al., US Patent 5,789,284 in view of Nakamura et al., US Patent 6,821,827 has been maintained for reasons of record.

The applied reference has a common Assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of

invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Yamazaki discloses the semiconductor method substantially as claimed. See figures 1A-9C, and corresponding text, where Yamazaki shows, pertaining to claim 10, a method of manufacturing a semiconductor device comprising the steps of: adding a metallic element **104** to a first semiconductor film **103** having an amorphous structure (figure 1A; col., 6, lines 9-23); crystallizing the first semiconductor film to form a first semiconductor film having a crystalline structure **105** (figure 1B; col. 6, lines 24-34); forming a barrier layer **106** on a surface of the first semiconductor film having a crystalline structure (figure 1C; col. 6, lines 43-58); forming a second semiconductor film **107** on the barrier layer (figure 1C; col. 6, lines 65-67); gettering the metallic element into the upper layer of the second semiconductor film to remove or reduce the amount of the metallic element within the first semiconductor film having a crystalline structure (figure1C-1D; col. 7, lines 10-15); and removing the second semiconductor film (figure 1D; col. 7, lines 56-67; col. 8, lines 1-10). In addition, Yamazaki shows, pertaining to claim 47, a method of manufacturing a semiconductor device comprising: forming a first semiconductor film **105** having an amorphous structure over a substrate **101** (figure 1A; col. 6, lines 9-23); providing the

first semiconductor film with a material **104** for promoting crystallization (figure 1A; col. 2, lines 50-55; col. 6, lines 1-8, 20-23); heating the first semiconductor film for crystallizing (figure 1B; col. 6, lines 24-34); irradiating the first semiconductor film with a laser light for improving crystallinity (col. 12, lines 28-44); forming a barrier layer **106** over the first semiconductor film having a crystalline structure (figure 1C; col. 6, lines 43-57); forming a second semiconductor film **107** over the barrier layer (figure 1C; col. 8, lines 27-35); gettering the material for promoting crystallization into the upper layer of the second semiconductor film (figure1C-1D; col. 7, lines 10-15). Also, Yamazaki shows, pertaining to claim 49, a method of manufacturing a semiconductor device comprising: forming a first semiconductor film **103** having an amorphous structure over a substrate **101** (figure 1A; col., 6, lines 9-23); providing the first semiconductor film with a material **104** for promoting crystallization (figure 1A; col. 2, lines 50-55; col. 6, lines 1-8, 20-23); heating the first semiconductor film for crystallizing (figure 1B; col. 6, lines 24-34); irradiating the first semiconductor with a laser light for improving crystallinity (col. 12, lines 28-44); forming a second semiconductor film over the first semiconductor film **107** (figure 1C; col. 8, lines 27-35); gettering the material for promoting crystallization into the second semiconductor film (figure1C-1D; col. 7, lines 10-15). Yamazaki shows, pertaining to claims 67 and 78, a method of manufacturing a semiconductor device comprising the steps of: providing a crystalline semiconductor film **105** comprising silicon over a substrate **101**, said crystalline semiconductor film containing a metallic element **104** (figure 1A; col., 6, lines 9-23); forming a barrier layer **106** over the crystalline semiconductor film (for claim 67, figure 1C; col. 6, lines 43-58); forming a semiconductor film **107** over the crystalline semiconductor film ; gettering the metallic element into the semiconductor film to remove or reduce the amount of the metallic

element within the crystalline semiconductor film (figure1C-1D; col. 7, lines 10-15). Also, Yamazaki shows, pertaining to claim 13,wherein the second semiconductor film is a semiconductor film having an amorphous structure or a crystalline structure. Yamazaki shows, pertaining to claim 15, wherein the metallic element is one element or a plurality of elements chosen for the group consisting of Fe, Ni, Co, Ru, Rh, Pd, Os, Ir, Pt, Cu and Au. In addition, Yamazaki shows, pertaining to claim 17, wherein the step of crystallizing the first semiconductor film is a heat treatment process. Also, Yamazaki shows, pertaining to claim 19, wherein the step of crystallizing the first semiconductor film is a process of irradiating strong light to the semiconductor film having an amorphous structure. Yamazaki shows, pertaining to claim 21, wherein the step of crystallizing the first semiconductor film is a heat treatment process and a process of irradiating strong light to the semiconductor film having an amorphous structure. In addition, Yamazaki shows, pertaining to claims 25, 53 and 71, wherein the step of forming a barrier layer is a step of oxidizing a surface of the (first, for claims 53 and 71) semiconductor film having a crystalline structure by irradiating ultraviolet light. Also, Yamazaki shows, pertaining to claim 27, wherein the step of gettering is a heat treatment process. Yamazaki shows, pertaining to claim 29, wherein the step of gettering is a process of irradiating strong light to the semiconductor film. In addition, Yamazaki shows, pertaining to claim 31, wherein the step of gettering is a heat treatment process and a process of irradiating strong light to the semiconductor film. Also, Yamazaki shows, pertaining to claims 33, 35, 37 and 39, wherein the strong light is emitted from a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. Yamazaki shows, pertaining to claim 43, wherein the third semiconductor film further comprises one element or a

plurality of elements selected from the group O, O_2, P, H, H_2. In addition, Yamazaki shows, pertaining to claims 63, 65 and 77, wherein the semiconductor device is applied to an electronic apparatus selected from the group consisting of a personal computer, a video camera, a mobile computer, a goggle type display, a DVD, a digital camera, a front type projector, a rear type projector, a mobile phone, and an electronic book.

Finally, Yamazaki shows, pertaining to claims 81-85, wherein the metallic element moves to the region of the second semiconductor film in a direction perpendicular to the first semiconductor film (figure 1C; col. 11, lines 40-50, ***Note***: the Examiner takes the position that since Yamazaki teaches that the metal element is absorbed into the second semiconductor film (amorphous silicon film) above the first semiconductor film (crystallized silicon film) the movement of the direction perpendicular to the first semiconductor film is obtained).

However, Yamazaki fails to show, pertaining to claims 10, 47, 49, 67, and 78-80, adding a noble gas element to an upper layer of the (second, for claims 10, 47 and 49) semiconductor film. In addition, Yamazaki fails to show, pertaining to claim 11, comprising the step of adding one element or a plurality of elements chosen from the group consisting of O, O_2, P, H and H_2 in addition to the noble gas element. Also, Yamazaki fails to show, pertaining to claims 41, 55, 57 and 73, wherein the noble gas element is at least an element selected from the group consisting of He, Ne, Ar, Kr and Xe. Finally, Yamazaki fails to show, pertaining to claims 45, 59, 61 and 75, wherein the second semiconductor film comprises the noble gas element at a concentration of 1×10^{19} to $1 \times 10^{22}/cm^3$.

Nakamura teaches, in figures 1A-25, and corresponding text, that the inert atoms, such as helium, neon, argon, krypton and xenon, in addition to phosphorous are implanted into a

crystallized semiconductor film for the purpose of creating gettering sites for the removal of impurities within a crystallized semiconductor film (col. 27, lines 13-31; col. 28, lines 3-35).

It would have been obvious to one of ordinary skill in the art to incorporate the follow: (1 adding a noble gas element to an upper layer of the (second) semiconductor film; (2 wherein the noble gas element is at least an element selected from the group consisting of He, Ne, Ar, Kr and Xe; (3 further comprising a step of adding one element or a plurality of elements chosen from the group consisting of O, O_2, P, H and H_2 in addition to the noble gas element; (4 wherein the second semiconductor film comprises the noble gas element at a concentration of 1 x 10^{19} to 1x $10^{22}/cm^3$, in the method of Yamazaki, pertaining to claims 10, 11, 41, 45, 47, 49, 55, 59, 61, 67, 73, 75, and 78-80, according to the teachings of Nakamura, with the motivation of creating gettering cites for the removal of impurities, such as, copper, nickel, silver, from the first semiconductor film, thereby dramatically improving the crystallized semiconductor film for an active region within a semiconductor device. In addition, it would be an advantage to use both a noble gas and an additional element for the purpose of creating a much more effective gettering technique. Finally, based on the combined teachings of Yamazaki in view of Nakamura, having a noble gas element concentration of 1 x 10^{19} to 1x $10^{22}/cm^3$ would result in routine experimentation, especially since no critically has been shown.

The rejection of claims 23, 51 and 69, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al., US Patent 5,789,284 in view of Nakamura et al., US Patent 6,821,827 in further view of Bhat et al., US Patent 6,291,888.

Yamazaki in view of Nakamura, discloses the semiconductor method substantially as claimed. See preceding rejection of claims 10, 13, 15, 17, 19, 21, 25, 27, 29, 31, 33, 35, 37, 39, 41, 43, 45, 47, 49, 53, 55, 57, 59, 61, 63, 65, 67, 71, 43, 75 and 77-80, under 35 U.S.C. 103(a).

However, Yamazaki in view of Nakamura, fail to show, pertaining to claims 23, 51 and 69, wherein the step of forming the barrier layer is a step of oxidizing a surface of the semiconductor film having a crystalline structure by using a solution containing ozone.

Bhat teaches, a thermal oxide film that may be formed by conventional techniques (col. 6, lines 12-15).

It would have been obvious to one of ordinary skill in the art to, incorporate, wherein the step of forming the barrier layer is a step of oxidizing a surface of the semiconductor film having a crystalline structure by using a solution containing ozone, in the method Yamazaki in view of Nakamura, pertaining to claims 23, 51 and 69, according to the teachings Bhat, with the motivation of creating an oxide film, whether the oxide film is formed by ozone or thermal oxidation, etc., would prove to be equivalent since the ultimate result would be to create an oxide film as a barrier layer.

Response to Arguments

Applicant's arguments filed 2/21/06 have been fully considered but they are not persuasive. In the Remarks on pages 19-25:

The Applicant raises the clear issue as to whether Yamazaki alone or in combination with Nakamura suggests or teaches adding a noble gas element to an upper layer of a semiconductor

film, especially since Yamazaki teaches the use of an amorphous silicon film as a gettering film and Nakamura teaches a different gettering film such as a crystallized silicon film.

The Examiner takes the position that the method of manufacturing a semiconductor device, as shown by Yamazaki (figures 1A-9C), and the implications made by Yamazaki, taken in combination with the solid teachings of Nakamura, would lead to one of ordinary skill in the art to substitute the noble gas element along with an additional element to form gettering sites within the second semiconductor layer. Specifically, Yamazaki teaches a first crystallized semiconductor film that includes a metallic element and then a barrier layer is formed on the surface of the first semiconductor film. Next, a second semiconductor film is formed on the barrier layer. The second semiconductor (amorphous silicon film) is then used as a gettering film to remove the impurities from the first semiconductor film. During this gettering process, the second semiconductor film (amorphous silicon film) is crystallized with the action of the metallic element being absorbed from the first semiconductor film (crystallized silicon film), as a result, a crystallized second semiconductor film is obtained (see col. 8, lines 27-35). It takes the teachings of Nakamura to realize the advantages to adding a noble gas element along with an additional element, thereby dramatically improving the crystallized semiconductor film for an active region within a semiconductor device. In addition, it would be an advantage to use both a noble gas and an additional element for the purpose of creating a much more effective gettering technique

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
April 21, 2006

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812